(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3301 Roll No. | | | | | | | | | |

B. Tech.

(Semester-I) Theory Examination, 2012-13

ELECTRONICS ENGINEERING

Time : 3 Hours] *[Total Marks : 100*

Note : Attempt questions from each Section as per instructions.

Section-A

Attempt *all* parts of this question. Each part carries 2 marks. 2×10=20

1. (a) Define A.C. resistance r_d of a diode. Derive its value in terms of η, V_T and I_{DQ}.

   (b) Explain the difference between avalanche and Zener breakdown in a *p-n* junction diode.

   (c) Define the pinch-off voltage V_p.

   (d) What do you understand by thermal runaway in BJT circuits.

(e) Draw the A.C. equivalent of OP-AMP circuit (i) practical (ii) ideal.

(f) Realize an Exclusive-OR gate using 2-input four NAND gates.

(g) Define α and β of a transistor and derive the relationship between them.

(h) Differentiate between :

(i) Positive and Negative logic systems

(ii) Analog and Digital Signals.

7. (i) What is the purpose of aquadag coating on the inside of the glass tube in a C.R.T.?

(j) State the working principle of digital multimeter.

Section-B

Attempt any *three* parts of this question. Each part carries 10 marks. 10×3=30

2. (a) (i) Derive the expression for ripple factor and rectification efficiency of half-wave and full-wave rectifiers.

(ii) Find the maximum and minimum current flowing through the Zener diode in Fig. 1.

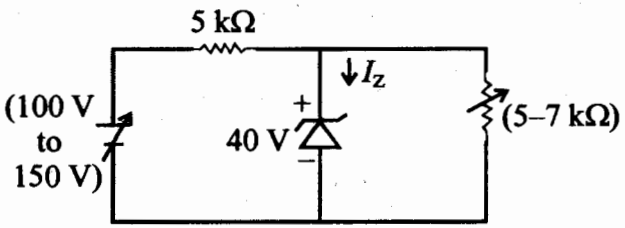

Fig. 1

(b) (i) What is self bias? Draw the circuit showing self bias of an NPN transistor in CE mode. Explain how self bias improves stability.

(ii) Consider the circuit shown in Fig. 2. Find the value of R_C required to obtain $V_C = 5V$.

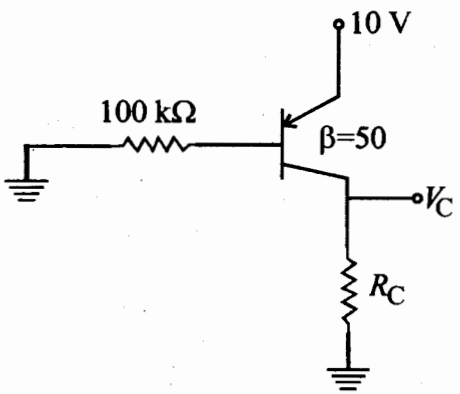

Fig. 2

Section-C

Attempt *all* questions of this Section. 10×5=50

3. Attempt any two parts :

(a) In the centre tap circuit shown Fig. 3 calculate :

(i) Average current

(ii) DC output voltage

(iii) DC output power

(iv) AC input power

(v) Rectifier efficiency. 5

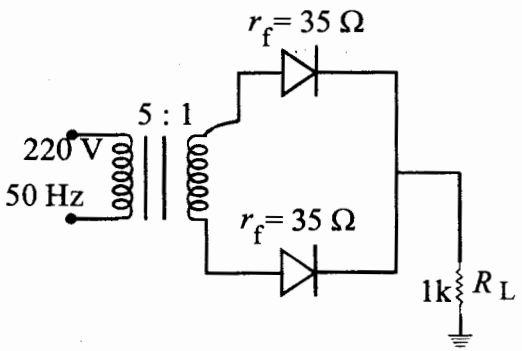

Fig. 3

(b) Determine V_0 for the network shown and input indicated in Fig. 4 and Fig. 5. 5

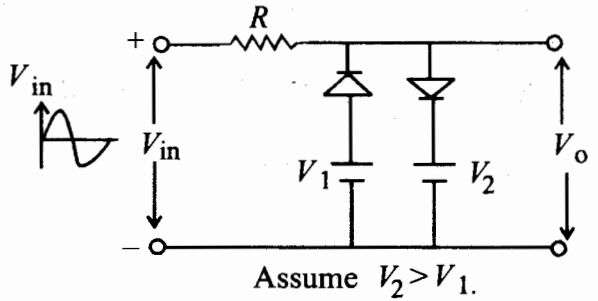

Fig. 4

7.

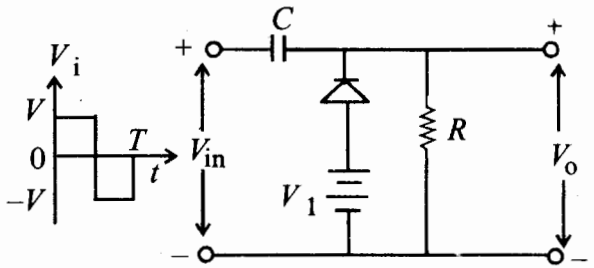

Fig. 5

(c) Explain the switching behaviour of a *p-n* junction diode when the input voltage changes from $+V_F$ to $-V_R$. Discuss how storage time can be reduced. 5

4. Attempt any two parts :

(a) Draw the *h* parameter equivalent circuit of the amplifier shown in Fig. 6. Calculate input impedance, current gain, voltage gain if $h_{ie} = 1\text{k}\Omega$ and $h_{fe} = 100$. 5

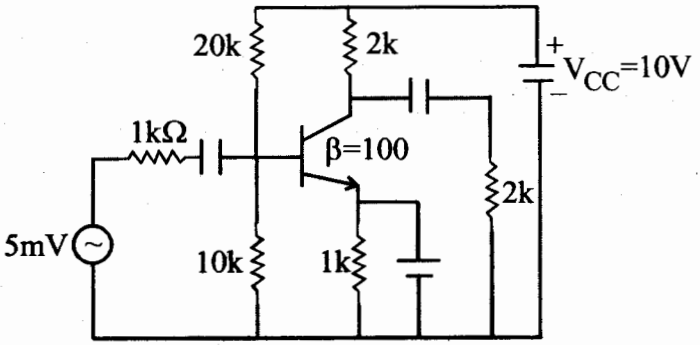

Fig. 6

(b) For an emitter follower, derive expressions for A_I, A_V, R_i and R_O. Compute these for $R_E = 5\,k\Omega$, $R_S = 1\,k\Omega$. Assume transistor parameters as : 5

$h_{ie} = 1\,k\Omega$, $h_{fe} = 100$, $h_{re} = 2\times10^{-4}$ and $h_{oe} = 20\,\mu A/V$.

(c) For a transistor in CE configuration :

(i) Derive an expression between I_C, I_B and I_{CO}.

(ii) Explain why slope of the output characteristics is more than in CB configuration.

(iii) Cutt-off condition. 5

5. Attempt any one part :

(a) For Fig. 7, given that the *n*-channel JFET has $I_{DSS} = 10\,mA$ and $V_P = -4$:

(i) Compute the Q point (I_{DQ}, V_{DSQ}), when $V_{GS} = -1.5$. Assume that it is biased in the pinch-off region.

(ii) Draw D.C. load line. 7

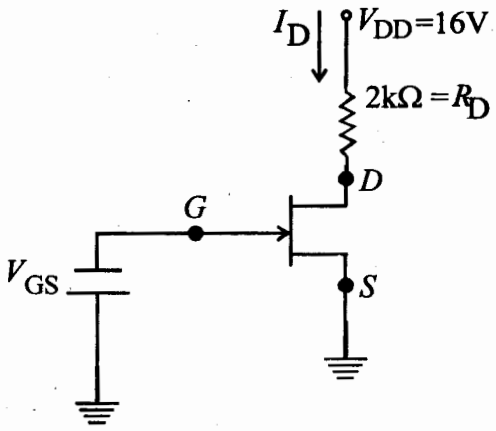

Fig. 7

(b) Define the following terms : 3

(i) CMRR

(ii) Slew Rate.

Or

(a) An n-channel JFET has $V_P = -5V$ and $I_{DSS} = 12$ mA and is used in circuit shown in Fig. 8. Find the operating point for the circuit. 4

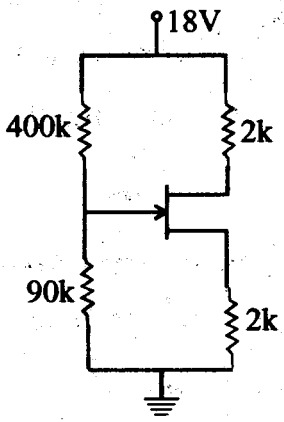

Fig. 8

(b) Explain : 6

(i) Ideal voltage transfer curve of OP-AMP.

(ii) Open loop OP-AMP configuration.

(iii) Closed loop OP-AMP configuration.

6. Attempt any one part :

(a) Use Karnaugh map to minimize following Boolean expression and express the result in (i) SOP form (ii) POS form :

$$Y = f(A, B, C, D)$$

$$= \Sigma(0, 1, 2, 6, 7, 10, 12, 15) + \Sigma d(3, 8, 13, 14).$$

Implement each expression using :

(i) NAND gates only

(ii) NOR gates only. 8

(b) Reduce the following Boolean expression using Laws of Boolean Algebra : 2

$$F = AB + A(B + C) + B(B + C).$$

Or

(a) Reduce the following Boolean expression : 5

$$[(AB)' + A' + AB]'[\{(AB)' + ABC\}(AB'C)]'.$$

(b) Find the value of x : 3

$$(786)_{10} = (x)_{16}.$$

(c) Convert $(82)_{10}$ to base 4 number system. 2

7. Write short notes on any two :

(a) Measurement of phase angle and frequency by a CRO 5

(b) Working Principle of CRO 5

(c) Basic control present in CRO. 5

(iii) Explain the phenomenon of "early effect" in a transistor.

(c) (i) Draw the structure of an *n*-channel depletion type MOSFET. Explain its working with the help of output drain characteristics and transfer characteristics.

(ii) By using an OPAMP, explain the operation of an integrator. What modifications are done to make it a practical integrator?

(d) (i) Given that $A = \overline{B}.C + B.\overline{C}$,then show that :

$$\overline{A} = B.C + \overline{B}.\overline{C} \text{ and}$$

$$C = \overline{A}.B + A.\overline{B} \cdot \quad 5$$

(ii) Convert the given expression into canonical POS form : 3

$$Y = A(A + \overline{B})(A + B + \overline{C}) \cdot$$

(iii) "Excess-3 code is a self complementary code." Explain. 2

(e) Sketch a CRT with electric focusing and deflection system. What are the main parts? Give the function of each part.